



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Technology Center 2600

Applicant: SARKINEN ET AL.

Examiner: Unknown

Serial No. 09/849,913

Group Art Unit: 2661

Filed: 05/04/01

Docket No. 1305.4US01

Title: METHOD AND APPARATUS FOR PROVIDING MULTI-PROTOCOL,
MULTI-STAGE, REAL-TIME FRAME CLASSIFICATION

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

3/12/02
David W. Lynch

Name

Signature

**Information Disclosure Statement
Under 37 C.F.R. §1.97(b)**

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant(s) respectfully submit(s) the items of information on the enclosed Form 1449 for the attention of the Examiner in the above-identified application.

This statement should be considered because it is filed before the mailing date of the first Office Action on the merits. Accordingly, no fee is due for consideration of the items listed on the enclosed Form 1449.

A copy of each document or other information listed on the enclosed Form 1449 is enclosed in accordance with 37 C.F.R. §1.98(a)(2) and/or a copy of each document is not provided because it was previously cited by or submitted to the U.S. Patent and Trademark Office in a parent application in accordance with 37 C.F.R. §1.98(d).

No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§102 and 103. In addition, Applicant(s) do(es) not represent that a reference

has been thoroughly reviewed or that any relevance of any portion of a reference is intended, and reserve the right to establish otherwise under 37 C.F.R. §1.131 or others.

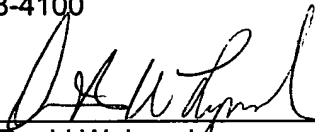
Consideration of the items listed is respectfully requested. According to M.P.E.P. §609, Applicant(s) request(s) that the Examiner return a copy of the attached Form 1449, marked as being considered and initialed by the Examiner, to the undersigned with the next official communication.

Authorization is hereby given to charge any additional fees or credit any overpayments that may be deemed necessary to Deposit Account Number 50-1038.

Respectfully submitted,

Altera Law Group, LLC
6500 City West Parkway, Suite 100
Minneapolis, Minnesota 55344-7701
952-253-4100

Date: 3/12/02

By: 
David W. Lynch
Reg. No. 36,204

DWL:tmj/ems

**INFORMATION DISCLOSURE STATEMENT**
PTO Form 1449

Docket Number 1305.4US01	Serial Number 09/849,913
Applicant(s) Sarkinen et al.	
Filing Date 05/04/01	Group Art Unit 2661

RECEIVED**MAR 22 2002****U.S. PATENT DOCUMENTS****Technology Center 2600**

EXAMINER INITIALS	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE (IF APPROPRIATE)
		6,175,568	01/16/01	Awdeh			
		6,167,445	12/26/00	Gai et al.			
		6,166,403	12/26/00	Castagnetti et al.			
		6,141,686	10/31/00	Jackowski et al.			
		6,136,638	10/24/00	Lee et al.			
		6,072,989	06/06/00	Witters et al.			
		6,047,002	04/04/00	Hartmann et al.			
		6,046,980	04/04/00	Packer			
		6,046,979	04/04/00	Bauman			
		6,032,190	02/29/00	Bremer et al.			
		5,995,439	11/30/99	Watanabe et al.			
		5,973,952	10/26/99	Crafts			
		5,943,481	08/24/99	Wakeland			
		5,923,596	07/13/99	Wu et al.			
		5,907,511	05/25/99	Crafts			
		5,901,095	05/04/99	Crafts			
		5,896,383	04/20/99	Wakeland			
		5,828,654	10/27/98	Takase et al.			
		5,812,476	09/22/98	Segawa			
		5,764,641	06/09/98	Lin			
		5,666,353	09/09/97	Klausmeier et al.			
		5,600,598	02/04/97	Skjaveland et al.			
		5,598,410	01/28/97	Stone			
		5,566,170	10/15/96	Bakke et al.			
		5,541,920	07/30/96	Angle et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	NO

OTHER DOCUMENTS

		"Frame Based ATM Over SONET/SDH Transport (FAST)," The ATM Forum, Technical Committee, fb-fbatm-0151.000, July 2000, 37 pgs.
		William Wong, "Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6798 , Retrieved June 15, 2001, 3 pgs.
		"Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6799 , Retrieved June 15, 2001, 2 pgs.

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		"Network Processors Take The High Road... And The Low Road," Electronic Design – July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6800 , Retrieved March 7, 2002, 3 pgs.
		"Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6802 , Retrieved June 15, 2001, 1 pg.
		"Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6804 , Retrieved June 15, 2001, 1 pg.
		"Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6806 , Retrieved June 15, 2001, 1 pg.
		"Network Processors Take The High Road... And The Low Road," Electronic Design, July 10, 2000, http://www.planetee.com/planetee/servlet/DisplayDocument?ArticleID=6808 , Retrieved June 15, 2001, 1 pg.
		"EZchip Technologies Completes Filing Patent Applications For Its 10/40G Network Processor Core Technology," EZchip – Press Release, June 8, 2000, http://www.ezchip.com/html/press_000918.html , printed January 22, 2001, 3 pgs.
		"7-Layer Packet Processing: A Performance Analysis, White Paper," EZchip, http://www.ezchip.com/html/tech_7layers.html , Retrieved January 22, 2001, 8 pgs.
		"Network Process Designs for Next-Generation Networking Equipment, White Paper," EZchip, http://www.ezchip.com/html/tech_nsppaper.html , Retrieved January 22, 2001, 8 pgs.
		"GILDER TECHNOLOGY REPORT," EZchip, September 2000, http://www.ezchip.com/html/gilder.html , Retrieved January 22, 2001, 2 pgs.
		"Putting Routing Tables in Silicon," IEEE NETWORK, Vol. 6, No. 1, January 1992, 11 pgs.
		Bossardt et al., "ABR Architecture and Simulation for an Input-Buffered and Per-VC-Queued ATM Switch," Department of Electrical and Computer Engineering, University of Illinois, 6 pgs.
		"C-5™ Digital Communications Processor," Product Brief, C-PORT, A Motorola Company, Date Unknown, 8 pgs.
		David Husak, "Network Processors: A Definition and Comparison," C-PORT, A Motorola Company, Date Unknown, 8 pgs.
		"Products," Applications, C-PORT, A Motorola Company, http://www.cportcorp.com/products/applications.htm , Retrieved January 23, 2001, 3 pgs.
		Husak et al., "Network Processor Programming Models: The Key to Achieving Faster Time-to-Market and Extending Product Life," C-PORT, A Motorola Company, May 4, 2000, 8 pgs.

Examiner:

Date Considered:

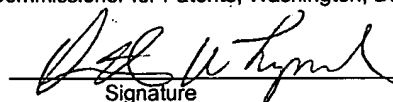


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Title: A METHOD AND APPARATUS FOR PROVIDING MULTI-PROTOCOL,
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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described herein, are being deposited in the United States Postal Service, as first class mail, with sufficient postage, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on 3/12/02

David W. Lynch
Name


Signature

Assistant Commissioner for Patents
Washington, D.C. 20231

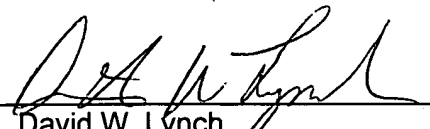
- ☒ Information Disclosure Statement, Form 1449, copies of forty-three reference(s)
- ☒ Transmittal Sheet
- ☒ Return postcard

Authorization is hereby given to charge any additional fees or credit any overpayments that may be deemed necessary to Deposit Account Number 50-1038.

Respectfully submitted,

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6500 City West Parkway, Suite 100
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Date: 3/12/02

By: 
David W. Lynch
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